**Innovation for Our Energy Future** 

## IEEE 1547.1 Overview

# IEEE P1547.1 Draft Standard for Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems

DOE High-Tech Inverter Workshop
Codes and Standards Development
October 13 – 14, 2004
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National Renewable Energy Laboratory

## **Presentation Outline**

- IEEE 1574.1
   Interconnection
   Test Std
- Test Procedure
   Validation



## IEEE 1547 Series

IEEE 1547-2003 - Standard for Interconnecting Distributed Resources with Electric Power Systems

This standard covers technical and testing requirements

IEEE 1547.1 – Draft Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems This standard has detailed test procedures for meeting the requirements in IEEE 1547

## IEEE 1547 Technical Requirements

#### General Requirements

- Voltage Regulation
- Integration with Area EPS Grounding
- Synchronization
- Secondary and Spot Networks

- Inadvertent Energizing of the Area EPS
- Monitoring
- Isolation Device

#### Response to Area EPS Abnormal Conditions

- Voltage Disturbances
- Frequency Disturbances
- Disconnection for Faults

- Loss of Synchronism
- Feeder Reclosing Coordination

#### Power Quality

- Limitation of DC Injection
- Limitation of Voltage Flicker
- Induced by the DR
- Immunity Protection
- Harmonics
- Surge Capability

Islanding

## IEEE Std 1547.1 (Conformance Test Procedures)

#### Scope

This standard specifies the Type, Production, and Commissioning tests that shall be performed to demonstrate that the interconnection functions and equipment of the DR conform to IEEE Std. 1547.

#### **Purpose**

Interconnection equipment that connects DR to an EPS must meet the requirements specified in IEEE 1547. Standardized test procedures are necessary to establish and verify compliance with those requirements. These test procedures must provide both repeatable results, independent of test location, and flexibility to accommodate the variety of DR technologies.

#### **Schedule**

- Draft 5.1 Issued summer 2004 for preparing ballot draft
- Plan to ballot P1547.1 Draft Standard in December 2004

## **IEEE Std 1547.1**

## Type (Design), Production and Commissioning Tests

#### 5.0 Type (Design) Tests

5.1 Temperature Stability

This test verifies that the interconnection equipment maintains measurement accuracy of parameters over its specified temperature range.

#### 5.2 Response to Abnormal Voltage

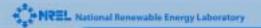
This test verifies that DR interconnection component or system ceases to energize the Area EPS as specified in IEEE 1547 with respect to overvoltage conditions. This test determines the magnitude and trip time for each overvoltage function.

## 5.3 Response to Abnormal Frequency

Same as Voltage except for abnormal frequency

#### 5.4 Synchronization

This test demonstrates the interconnection equipment will accurately and reliably synchronize to the Area EPS according the requirements of IEEE 1547. Two basic test methods are provided: Method 1 verifies that a synchronization control function will cause the paralleling device to close only when key synchronization parameters are within allowable limits; Method 2 determines the magnitude of the synchronization startup current.



## **IEEE Std 1547.1 Interconnection Tests**

#### 5.0 Type (Design) Tests

#### 5.5 Interconnection Integrity

These tests includes 1) Protection From Electromagnetic Interference (EMI), 2) Surge Withstand Performance, and a 3) dielectric test on the paralleling device. These tests are based on protocol in IEEE C37.90.1, C37.90.2, C62.41.2, and C62.45.

#### 5.6 DC injection

This test verifies that an inverter-based DR system complies with the DC current injection limit specified in of IEEE 1547.

#### 5.7 Unintentional Islanding

This test provides a means to determine that a DR or its interconnection system will cease to energize the connection with the Area EPS when an unintentional island condition is present. This test is currently based on matching the DR output to a resonant load.

#### 5.8 Reverse Power

Since one of the ways in which DR often meet the unintentional islanding requirement is to use a reverse or minimum power relay, this test is performed to characterize the accuracy of the reverse-power protection magnitude setting(s) of the interconnection equipment.



## **IEEE Std 1547.1 Interconnection Tests**

#### 5.0 Type (Design) Tests

5.9 Cease to Energize Functionality and Loss of Phase

This test verifies that DR interconnection system ceases to energize the Area EPS as specified in IEEE 1547 with respect to individual open phase conditions.

#### 5.10 Reconnect Time

This test verifies the functionality of the DR interconnection component or system reconnect timer, which delays the DR reconnection to the Area EPS following a trip event.

#### 5.11 Harmonics

This test measures the individual current harmonics and total demand distortion (TDD) of the DR interconnection component or system under normal operating conditions and see that they are within the limits of IEEE 1547.

#### 5.12 Flicker

No specific type test procedures since flicker is site dependent

## **IEEE Std 1547.1 Interconnection Tests**

#### 6 - Production Tests

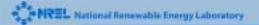
Production tests verify the operability of every unit of interconnect equipment manufactured for customer use.

- Response to Abnormal Voltage
- Response to Abnormal Frequency
- Synchronization

#### 7 - Commissioning Tests

Commissioning tests are conducted after the interconnection system is installed and is ready for operation.

- Verification and Inspections
- Field Conducted type and Production Tests



## **IEEE Std 1547.1 Tests**

### incorporated into UL1741 for product pre-certification

## NREL Interconnection Pre-Certification Approach

#### **IEEE 1547**

## Interconnection System Requirements

- Voltage Regulation
- Grounding
- Disconnects
- Monitoring
- Islanding

#### IEEE 1547.1

- InterconnectionSystem Testing
- •O/U Voltage
- and Frequency
- Synchronization
- •FMI
- Surge Withstand
- DC injection
- Harmonics
- Islanding
- Reconnection

#### UL 1741

## Interconnection Equipment

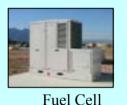
- Construction
- Protection against risks of injury to persons
- Rating, Marking
- Specific DR Tests for various technologies

## Interconnection Testing

## **Distributed Energy** Resources



## **Electric Power Systems**





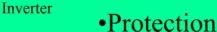


PV

**Functions** 







DER and Load Control

Ancillary Services

Communications

Metering







Wind



Energy Storage



Switchgear, Relays, & Controls





**Utility** 

Grid

**Local Loads Load Simulators** 

**Utility Grid Simulator** 

**Micro Grids** 

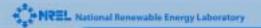




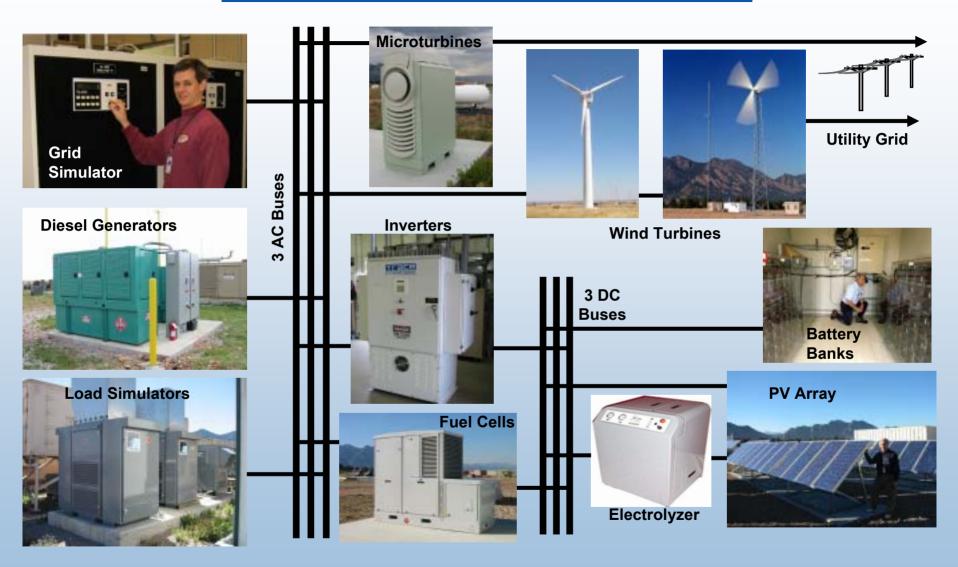


## **Testing Summary**

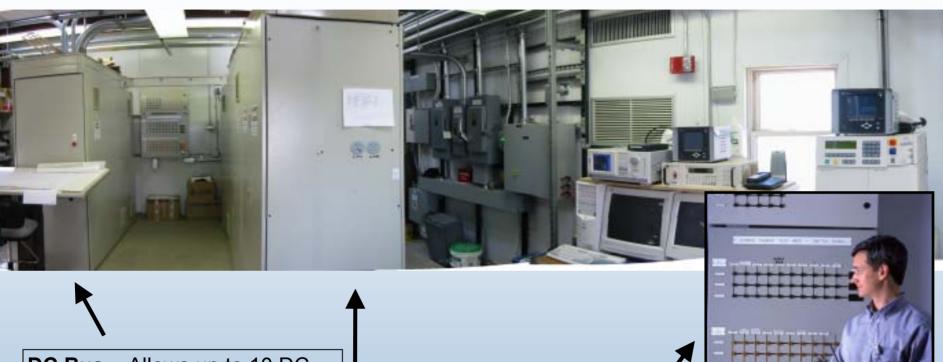
- This presentation outlines some of the specific interconnection tests being validated for inclusion in IEEE 1547.1.
- Generic monitoring, measurement, and testing strategies could be useful in P1547.1. The file size, sampling rate, and correct sampling window were significant factors of testing that could be mentioned in P1547.1. Advice and warnings of issues to be aware of to aid smooth and accurate testing should also be included.
- Some values from the earlier draft of P1547.1 standard were incompatible with the testing setup and will need modification. This information has been passed on to members of the IEEE P1547.1 working group for revision in future drafts.
- Care must be taken to test each parameter individually without other protective functions operating.
- For More Information and Copies of the full testing reports go to www.eren.doe.gov/distributedpower or www.nrel.gov



## **NREL Testing Capabilities**



## **NREL Testing Capabilities**



**DC Bus** – Allows up to 10 DC device (Battery, PV) connections

**AC Bus** (3Phase, 480V, 400A rated) – Allows up to 15 AC device (inverters, microturbine, generators) connections

Switch Panel – Computer controlled. Allows tester to easily configure systems. Ability to run 3 independent systems simultaneously.



## Interconnection Equipment Testing Examples

GE Universal Interconnection Technology (UIT)





ASCO - Soft-Load Transfer Switch



Validation of IEEE P1547 Interconnection Standard Tests

- Over/Under Voltage and Frequency Response
- Unintentional islanding test

## **Test Results – System Configuration**



200kW Grid Simulator



Transfer Switch





Programmable Load Banks



## <u>Test Results – IEEE 1547 Response Times</u>

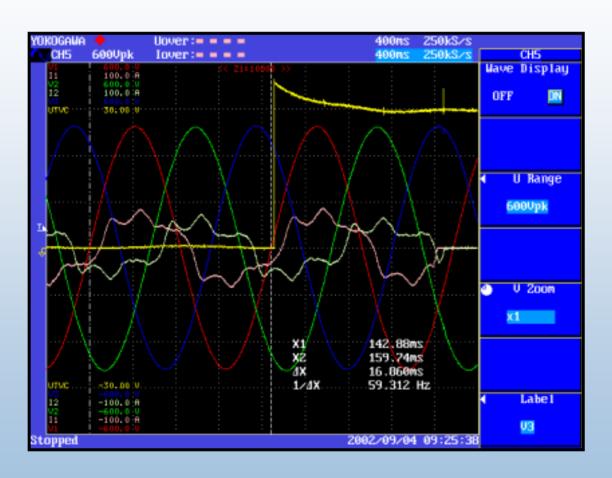
#### **Response to Abnormal Voltage**

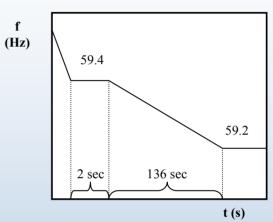
Voltage Range (Based on 480 V)	Clearing Time (s)
V<240	0.16
240≤V<422.4	2
528 <v<576< td=""><td>1</td></v<576<>	1
V≥576	0.16

#### **Response to Abnormal Frequency**

DR SIZE	Frequency Range (Hz)	Clearing Time (s)	
≤30	>60.5	0.16	
kW	<59.3	0.16	
	>60.5	0.16	
>30 kW	<{59.8–57.0} (adjustable setpoint)	Adjustable 0.16–300	
	<57.0	0.16	

Testing Results from ASCO SLTS – Underfrequency Magnitude Test

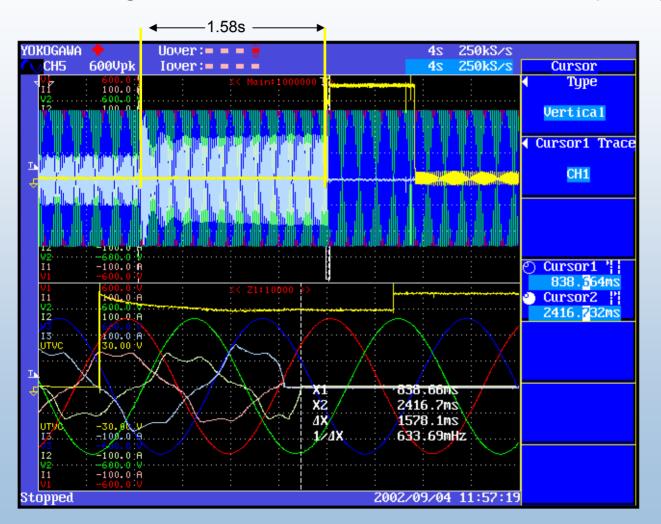


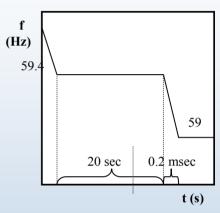


**Table 1. Underfrequency Magnitude** 

Underfrequency Magnitude			
•	Trip Frequency		
1	59.301		
2	59.311		
3	59.298		
4	59.312		
5	59.284		
Average	59.301		
Setting	59.3		

Testing Results from ASCO SLTS – Underfrequency Time Test





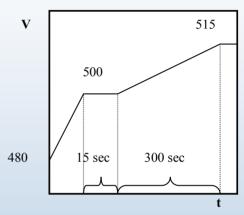
**Underfrequency Time** 

Underfrequency Time			
Trial Number	Trip Time (s)		
1	1.58		
2	1.48		
3	1.58		
4	1.57		
5	1.54		
Average	1.55		
Required	1.70		



Testing Results from ASCO SLTS – Overvoltage Magnitude Test



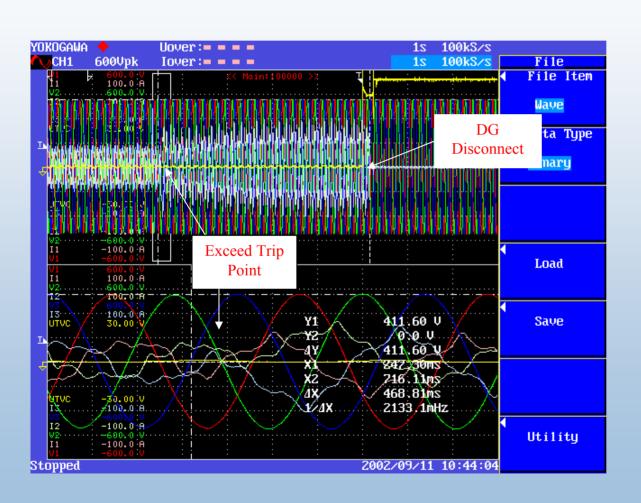


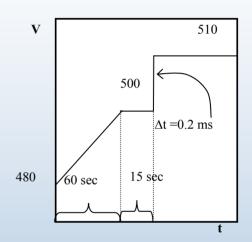
#### Overvoltage Magnitude

Overvoltage Magnitude			
Trial Number	Trip Voltage		
1	504.300		
2	502.500		
3	504.700		
4	504.600		
5	504.150		
Average	504.050		
Setting	504.0		



Testing Results from ASCO SLTS – Overvoltage Time Test



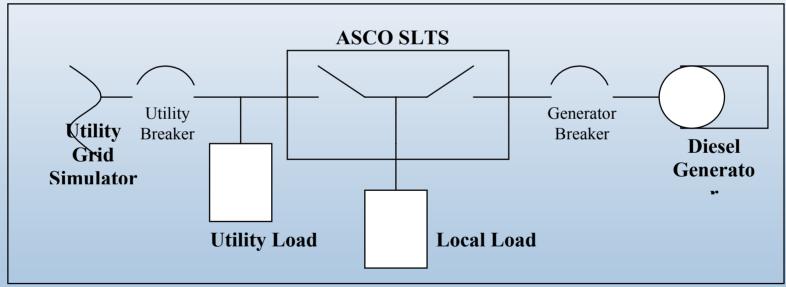


#### **Overvoltage Time**

Overvoltage Time			
Trial Number	Trip Time (s)		
1	0.436		
2	0.428		
3	0.378		
4	0.396		
5	0.468		
Average	0.421		
Required	1.00		

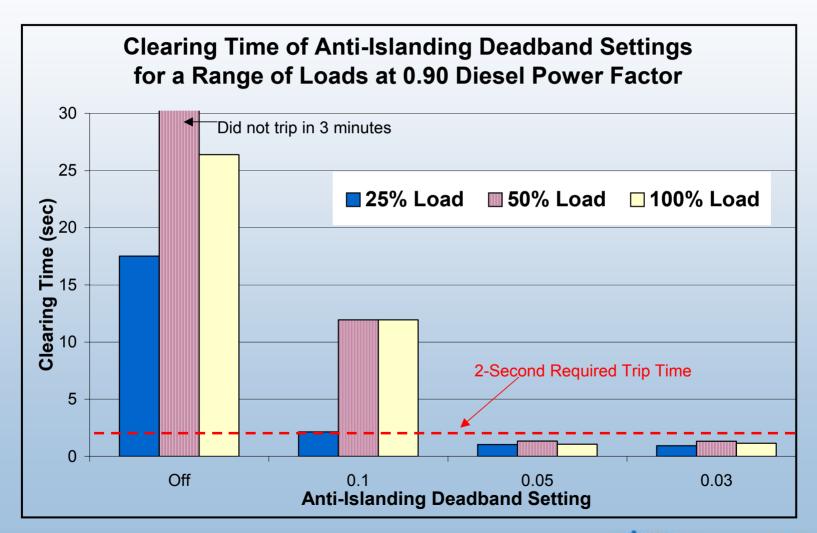


- Testing Results from ASCO SLTS Unintentional Islanding
- IEEE 1547 requirement is to disconnect within 2 seconds of island formation



Anti-islanding test setup

Testing Results from ASCO SLTS – Unintentional Islanding



## **Testing Results – GE UIT**

Size of Non-Detect Zone (NDZ) reduces as power level increases

Results from anti-islanding NDZ testing.					
DG output (kW)	Active Load (kW)	Reactive Load ( kVAR)	Power Mismatch (kW)	NDZ Size (% of P <sub>DG, nom</sub> )	
20	23	36	3	2.4	
35	37.5	62.5	2.5	2.0	
50	51.25	90	1.25	1.0	
80	81.5	144	1.5	1.2	

Paculte from anti-islanding ND7 testing

Examine the effects of switching in load while the DG was islanded and supplying a local load. That is, after the DG and load islanded (without being detected), how much load step would cause the island to be detected.

The test showed that steps less than 0.8% transient power would not cause the DG to trip.

Using small DG steps, the DG would continue to remain connected even if total change is much larger (up to rating of DG).